WOORIRO EYESAFE LASER RangeFinder RECEIVER

MODEL : WDR120

General Description

The Model WDR120 eye-safe LADAR receiver is designed for laser rangefinding and surveying. It features an InGaAs APD, ensuring both eye safety and high sensitivity. A CMOS IC is integrated to enhance performance and compactness. The use of a single FR4 PCB and a standard TO-8 package provides a cost-effective solution for LADAR receivers..

Features

- 6ns~28ns input pulse
- InGaAs APD chip
- Integrated CMOS TIA
- Providing TPG(Time Programmed Gain) mode
- Internally adjusted and temperature compensated APD bias
- Standard TO-8, FR4 PCB
- Single 12V power supply except APD bias

Applications

- LADAR receiver

Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings *(T_C=25°C, unless otherwise specified)*

Parameter	Symbol	Rating	Unit
TIA supply voltage	V_{DD}	+13	V
Optical input power	P_{opt}	1	mW
Operating case temperature range	T_C	-32 to +64	℃
Storage temperature range	T_{STG}	-55 to +125	℃

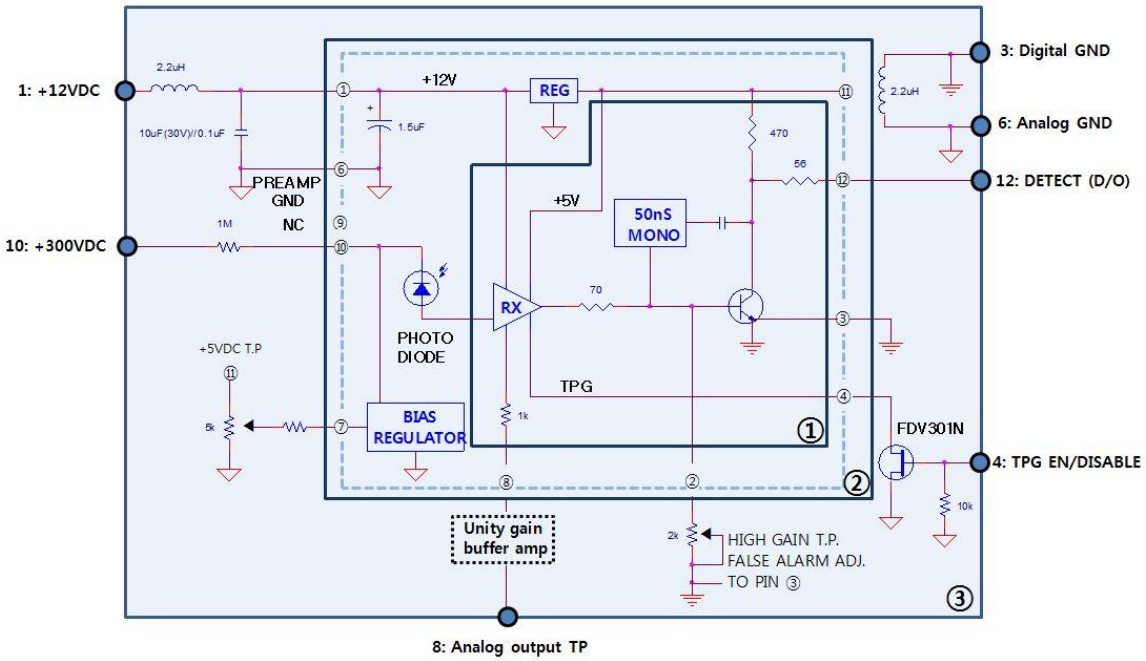
Electro-Optical Characteristics

Inspection sheet shall be appended to products when they are delivered. Test report shall be submitted in papers and in electronic media. It shall contain the major in following items.

Table 2. Electro-Optical Characteristics *(T_C=25°C, unless otherwise specified)*

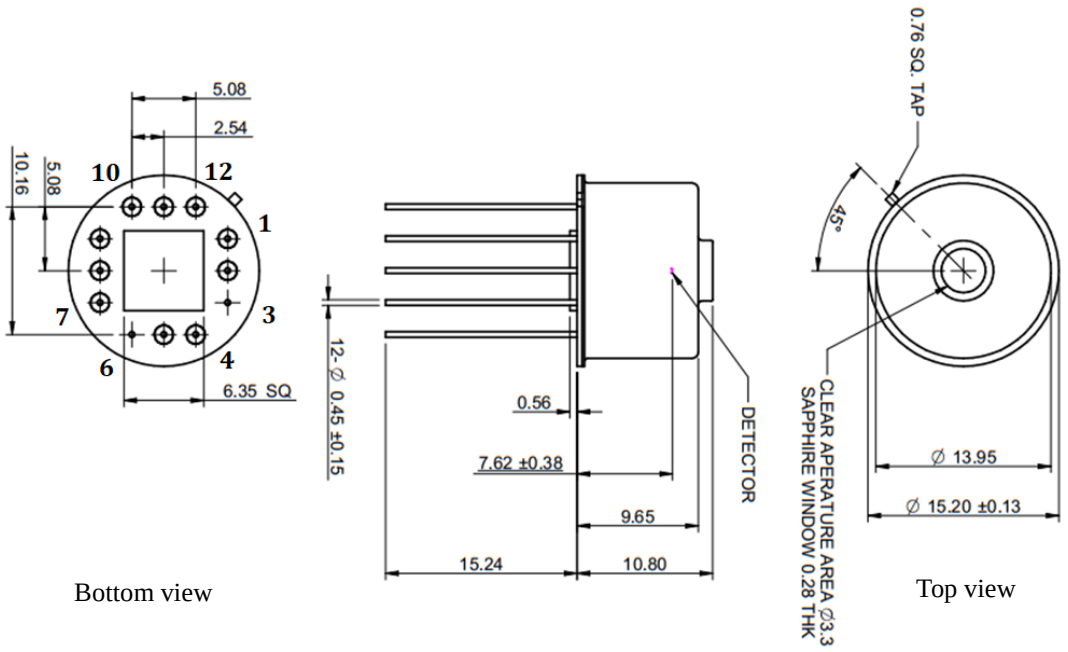
Parameter		Performance	Condition
Type		Hybrid	
PD	Type	InGaAs APD	
	Receiving diameter	200um	
	Leakage current	Compensated	
	Operating Wavelength	1250~1640nm	
Sensitivity		3 nW typ 8 nW max	1540nm, 28ns pulse, 50% detection, 0.1% FAR
Output Pulsewidth		55 ns typ	TTL or CMOS level Negative logic FWHM(Full Width at Half Maximum) Oscilloscope Load = 1㏁//12pF
Time Programmed Gain (TPG)		27dB min	2V or open enables TPG. 0V or GND inhibits TPG and holds low gain.
Current consumption		25mA typ 35mA max	

Functional Diagram



① Integrated chip ② PCB module unit ③ Recommanded Evaluation board circuit for application

Mechanical Dimension



Bottom view

Top view

Pin Configuration

Table 3. PIN Configuration

Pin #	Signal Name	Function
1	+12V	+12VDC power input
2	HIGH GAIN T.P	2kΩ Adjust TH (FAR) using variable resistance.
3	START/STOP RTN	Digital ground and connected to PIN6.
4	-INHIBIT TPG	Maximum gain mode when open or high. Minimum gain mode at pull-down.
5	PREAMP Output INTERCONNECT	Disabled.
6	PREAMP GND	Analog ground and connected to PIN.3.
7	APD BIAS ADJUST	Adjust APD Bias using 5kΩ variable resistance.
8	PREAMP T.P.	TP used for Optical alignment of the detector, for checking amplifier output.
9	NO CONNECTION	Disabled.
10	+H.V. I/P	High voltage input for APD bias voltage.
11	+5V T.P.	TP for internal +5V verification.
12	START/STOP	50 ns negative pulse output upon optical signal detection.

Precautions for Use

This device is susceptible to damage as a result of ESD(electrostatic discharge). Use of ground s traps, anti static mats, and other standard ESD protective equipment is recommended when handl ing or testing this device. Soldering temperature of the leads should not exceed 350℃ for more t han 10 seconds.

Specifications described here are subject to change without notice